What is claimed is:

1. A method of estimating modulation noise for use in a transmitter having a phase locked loop, said method comprising the steps of:

calculating an average of historical samples of phase error samples produced by said phase locked loop;

subtracting said average from a current phase error sample to yield a normalized phase error;

generating an exception event if said normalized phase error exceeds a threshold; and

repeating said steps of calculating, subtracting and generating over a period of time and outputting a failure indication if the number of exception events exceeds a maximum criteria and a pass indication otherwise.

2. The method according to claim 1, wherein said step of calculating comprises the step of calculating a moving average over a plurality of historical phase error samples.

3. The method according to claim 1, wherein said threshold is configurable.

4. The method according to claim 1, wherein said maximum failure criteria is configurable.

5. The method according to claim 1, wherein said period of time is configurable and corresponds to the number of symbols to be considered in estimating said modulation noise.

6. The method according to claim 1, further comprising the step of decimating said phase error samples before said step of calculating.

7. The method according to claim 1, adapted to be implemented in testing software residing in an integrated on-chip processor such that the need for external software/hardware is substantially eliminated.

8. The method according to claim 1, wherein said phase error samples comprise filtered phase error samples.

9. The method according to claim 1, wherein said transmitter is compliant with a Bluetooth standard.

10. The method according to claim 1, wherein said transmitter is used in a wireless communications network.

11. The method according to claim 1, wherein the phase locked loop comprises a digital phase locked loop.

12. The method according to claim 1, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

13. The method according to claim 1, adapted to be implemented in a Field Programmable Gate Array (FPGA).

14. An apparatus for estimating modulation noise for use in a transmitter having a phase locked loop, comprising:

means for calculating an average of historical samples of phase error samples produced by said phase locked loop;

means for subtracting said average from a current phase error sample to yield a normalized phase error;

means for generating an exception event if said normalized phase error exceeds a threshold; and

means for repeating said functions of calculating, subtracting and generating over a period of time and outputting a failure indication if the number of exception events exceeds a maximum criteria and a pass indication otherwise.

15. The apparatus according to claim 14, wherein said mean for calculating comprises means for calculating a moving average over a plurality of historical phase error samples.

16. The apparatus according to claim 14, wherein said threshold is configurable.

17. The apparatus according to claim 14, wherein said maximum failure criteria is configurable.

18. The apparatus according to claim 14, wherein said period of time is configurable and corresponds to the number of symbols to be considered in estimating said modulation noise.

19. The apparatus according to claim 14, further comprising means for decimating said phase error samples before said average is calculated.

20. The apparatus according to claim 14, adapted to be implemented in testing software adapted to execute on an on-chip software based processor.

21. The apparatus according to claim 20, wherein said testing software is stored in rewritable memory wherein said testing software is replaced by normal operation software once testing is complete.

22. The apparatus according to claim 14, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

23. The apparatus according to claim 14, adapted to be implemented in a Field Programmable Gate Array (FPGA).

24. An apparatus for estimating modulation noise in a transmitter, comprising:

first means for estimating frequency deviation errors of a signal output from said transmitter utilizing measurements of a phase error signal observed within a phase locked loop in said transmitter;

second means for comparing a plurality of phase error signal samples over a period of time to a threshold and generating an exception event each time a phase error signal sample exceeds said threshold; and

generating a failure indication if the number of exception events exceeds a criteria and generating a pass indication otherwise.

25. The apparatus according to claim 24, wherein said phase error signal comprises a digital sample.

26. The apparatus according to claim 24, wherein said phase error signal comprises an analog sample.

27. The apparatus according to claim 24, wherein said threshold is configurable.

28. The apparatus according to claim 24, wherein said criteria is configurable.

29. The apparatus according to claim 24, wherein said period of time is configurable.

30. The apparatus according to claim 24, wherein said threshold is configured to correspond to a particular noise threshold on a modulation noise probability density function.

31. The apparatus according to claim 24, wherein lowering said threshold causes the number of exception events to increase for the same criteria and period of time and increasing said threshold causes the number of exception events to decrease for the same criteria and period of time.

32. The method according to claim 24, adapted to be implemented in testing software adapted to execute on an embedded microprocessor or digital signal processor.

33. The apparatus according to claim 32, wherein said testing software is stored in rewritable memory wherein said testing software is replaced by normal operation software once testing is complete.

34. The apparatus according to claim 24, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

35. The apparatus according to claim 24, adapted to be implemented in a Field Programmable Gate Array (FPGA).